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(71) Applicant: SHIN-ETSU HANDOTAI COMPANY, LIMITED
4-2, Marunouchi 1-Chome
Chiyoda-ku Tokyo(JP)

Applicant: NAOETSU ELECTRONICS COMPANY
596-2, Oaza Jonokoshishinden Kubiki-Mura
Nakakubiki-gun Niigata-Ken(JP)

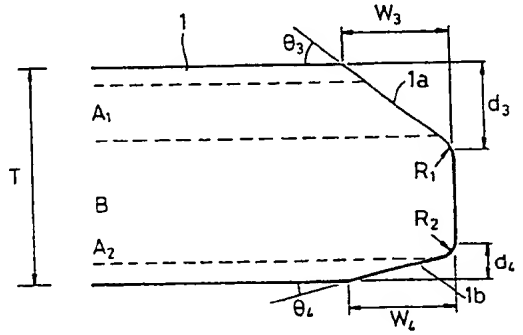
(72) Inventor: Kimura, Hirokazu, c/o Naoetsu Electronics Co.
596-2, Ooaza Jonokoshishinden, Kubiki-mura
Nakabuki-gun, Niigata(JP)

(74) Representative: Perry, Robert Edward et al
GILL JENNINGS & EVERY 53-64 Chancery Lane
London WC2A 1HN(GB)

(54) Method of processing substrate for semiconductor device.

(57) A substrate suitable for use in a semiconductor device is prepared by subjecting the impurities in a substrate (1) at a lower concentration to diffusion, to form a more concentrated impurity layer at the opposed surfaces, and part of the thickness of the substrate is removed to expose a layer doped with the impurity at the lower concentration on one surface (B). The thus exposed surface is polished to provide the producting, having a varying concentration of impurities. The edges are bevelled at different angles ($\theta\theta$), before or after diffusion.

FIG.1



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METHOD OF PROCESSING SUBSTRATE FOR SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method of processing a substrate for semiconductor device, and more specifically, to a method of beveling the substrate.

Description of the Related Art

Conventionally, a substrate for semiconductor device has been beveled so that the circumferential edges of the front and back surfaces thereof is made substantially symmetrical. This beveling process is usually carried out using a diamond grindstone having a U- or V-shaped groove edge provided around the outer circumference thereof in such a manner that the diamond grindstone is brought into contact with the substrate for semiconductor device and they are rotated about axes disposed in parallel each other, and thus the periphery of the substrate for semiconductor device is formed to a wedge-shaped cross section. Since the wedge-shaping is performed by the beveling process, it is called a beveled portion, which is relatively smaller in size in the case of a discrete semiconductor substrate as compared with that of a semiconductor substrate for integrated circuits (IC) and mainly intends to prevent the substrate for semiconductor device from being chipped off while it is handled in the fabrication of IC.

This beveling is usually carried out in the fabricating processes of a substrate for semiconductor device just after a semiconductor monocrystal has been cut or after it has been further subjected to a lapping process. The beveling process is carried out at a relatively earlier stage of the fabricating process of the substrate for semiconductor device, because a grindstone having a grinding layer composed of relatively coarse fixed abrasive grains is used in the process, and thus the substrate is greatly damaged and coarse isolated grains are produced during the beveling process.

A semiconductor discrete device is fabricated by a triple diffusion method, wherein, first, a substrate for semiconductor device cut off from a monocrystal is subjected to a grinding and/or etching process, and the dopant to form a collector region is diffused into the bulk of the substrate through both the surfaces at an elevated temperature. Next, about a half of the thickness of the substrate is ground and removed (hereinafter, referred to as half-off) from only one surface thereof, the inner low concentrated impurity layer (same as the impurity species and concentration of the monocrystal) of the substrate is exposed, the substrate is ground while accurately controlling the thickness (usually, referred to as x_1) of the low impu rity layer, and further diffusions for base and emitter regions are performed through limited openings on the exposed surface to finally obtain the semiconductor discrete device. Since the beveling process is carried out to the substrate before it is subjected to diffusion or after it has been subjected thereto in the fabricating processes of the semiconductor discrete device, a technical problem arises in a conventional beveling method.

Prior art will be described based on the description of, for example, Japanese Examined Patent Publication No. 60-58579.

Figure 3 shows a substrate 21 for semiconductor device having unsymmetrical beveled portions 21a and 21b respectively formed on the front and back surfaces thereof. The beveled portions 21a and 21b are formed using a rotary grindstone 22 shown in Figure 4.

The beveled portion 21a and 21b of the substrate 21 for semiconductor device are arranged as follows. Assuming that the beveled portion 21a on the surface of the substrate from which a diffused layer has been ground and removed (hereinafter, referred to as a front surface) has a beveled width w_1 and a beveled depth of d_1, and the beveled portion 21b on the back surface has a beveled width w_2 and a beveled depth d_2, an arrangement is such that w_1 w_2, d_1 d_2, and the angle θ_1 between the inclining surface and the main surface of the beveled portion 21a of the front surface [θ_1 = arc tan(d_1/w_1)] is equal to the angle θ_2 between the inclining surface and the main surface of the beveled portion 21b of the back surface [θ_2 = arc tan(d_2/w_2)]. Note that, in this case, the beveled width w_2 of the beveled portion 21b of the back surface must be set to a prescribed value or a value larger than it to prevent the substrate 21 for semiconductor device from being chipped off through handling.

According to this technology, a part of the beveled portions 21a and 21b is left on the front and back surfaces of the substrate 21 for semiconductor device even after the front and back surfaces of the substrate 21 for semiconductor device have been lapped to the levels A_1 and A_2 which are shallower than the beveled depths d_1 and d_2, the front surface has been removed (half-off) to the surface B which is shallower than the beveled depth d_2, and then the substrate has been polished, whereby the chip-off of the substrate 21 for

semiconductor device can be effectively prevented in the following process.

Nevertheless, the following problems arise in the prior art.

The beveled angle θ_1 of the front surface must be a prescribed value or a value less than it, because the beveled depth d_1 of the front surface is made large so that a part of the beveled portion 21a is left after the substrate has been subjected to the half-off and polishing, and further the beveled portion 21b of the back surface has the beveled width w_2 which is set to a prescribed value or a value larger than it, as described above. Under these circumstances, if the beveled angle θ_1 of the front surface and the beveled angle θ_2 of the back surface are set to the same value, as described above, the wedge-like periphery of the substrate is made considerably sharp. As a result, the circumferential edge of the substrate 1 for semiconductor device are liable to be chipped off.

Further, according to the substrate 21 for semiconductor device of the above technology, the beveled widths w_1 and w_2 of both the surfaces must be differently formed, and thus when a substrate 41 for semiconductor device (numeral 41 is used to discriminate this substrate from the substrate 21 for semiconductor device to which the beveled portions 21a and 21b have been formed) is processed to form the beveled portions 21a and 2lb, as shown in Figure 4, in such a manner that they are simultaneously formed by a grindstone 22 having the grinding surface which contour is predetermined to conform with the dimensional requirements of the periphery of the beveled substrate 21 for semiconductor device, the corner of the front surface having the larger beveled width is first abutted against the grinding surface 22a of the grindstone 22. Thereafter, the corner of the back surface having the smaller beveled width is next abutted against the grinding surface 22c of the grindstone 22. As a result, downward pressure from the grinding surface 22a is left not neutralized until after the corner of the front surface has gone toward the grinding surface 22a and the corner of the back surface is abutted against the grinding surface 22c. Therefore, the substrate 21 for semiconductor device is sometimes chipped off while it is in a beveling process.

SUMMARY OF THE INVENTION

It is an object of the present invention, which has been achieved taking into consideration the above problems arisen particularly in a beveling method applied to a substrate for semiconductor device to which collector diffusion has been finished or is not finished, that is, the substrate for a power transistor by so called the triple diffusion method, to provide a method of processing a substrate for semiconductor device capable of effectively preventing the substrate from being chipped off.

Other objects and novel advantages of the present invention will be apparent from the following description and accompanying drawings of this specification.

To achieve the above object, according to one aspect of the present invention, before both surfaces of a substrate for semiconductor device is subjected to diffusion or after they have been subjected thereto, beveled portions are formed to have such a contour of the periphery of the substrate as a beveled depth of the surface to be half-offed (hereinafter, referred to as a front surface) of the substrate is made larger than that of the surface (hereinafter, referred to as a back surface) of the substrate, and an angle between an inclining surface and a main surface of the beveled portion of the front surface is made larger than that of the beveled portion of the back surface.

Further, according to another aspect of the present invention, the respective angles of the substrate mentioned above are set such that the front and back surfaces have substantially the same width.

Further, according to further aspect of the present invention, the beveled portions on the front and back surfaces are simultaneously formed by a grindstone having the grinding surface corresponding to the profile of the periphery of the substrate which is formed after the substrate has been processed.

According to the present invention, since beveled portions are formed to have such a peripheral contour of the substrate as the angle between the inclining surface and the main surface of the beveled portion on the front surface is made larger than that of the beveled portion on the back surface, and a beveled depth of the front surface side is made larger than that of the back side surface, the strength of the circumferential edges is increased, whereby the substrate for semiconductor device is effectively prevented from being chipped off when it is in a beveling process itself. Further, there is an advantage in that when both surfaces of the substrate is successively subjected to diffusion, the occurrence of the chip-off of the substrate is greatly prevented in the handling of the substrate in the diffusion, or in the handling thereof when about a half of the front surface of the substrate is removed.

Furthermore, since the beveled substrate for semiconductor device has the beveled portion properly left after half-off at the circumferential edge of the front surface thereof to prevent the

substrate from being chipped off in the following process, the front surface has the same effect as that of the back surface.

Further, since the beveled portions formed on both main surface of the substrate have the same beveled width, the beveled portions of the front and back surfaces can be simultaneously formed by a grindstone having the grinding surface corresponding to the profile of the periphery of the substrate which is formed after the substrate has been processed. In this case, since the corners of the front and back surfaces are simultaneously abutted against the grinding surface of the grindstone, whereby the grinding opera tion of the substrate is simultaneously carried out and finished at both the edges. As a result, while the beveled portions are ground, pressure originated from one of the grinding surfaces being ground is always counterbalanced by that from the other grinding surface being ground, whereby the occurrence of strain due to grinding and the chip-off of the substrate for semiconductor device can be prevented during the operation.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram showing the circumferential portion and the vicinity thereof of an embodiment of a substrate for semiconductor device according to the present invention;

Figure 2 is a diagram showing a substrate for semiconductor device and the vicinity of the grinding surface of a grindstone used to bevel off the circumferential edge of the substrate for semiconductor device; and

Figure 3 is a diagram showing the circumferential portion and the vicinity thereof of an embodiment of a conventional substrate for semiconductor device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An example of a method of processing the periphery of a substrate for semiconductor device according to the present invention will be described below with reference to draw ings.

Figure 1 shows the state of the substrate for semiconductor device of the embodiment before it is subjected to a half-off process.

In the figure, numeral 1 designates the substrate for semiconductor device, and beveled portions 1a and 1b are formed around the circumferential edges thereof. The substrate 1 for semiconductor device can be, for example, an intermediate member of a substrate used to form a discrete semiconductor device having the beveled portions 1a and 1b arranged unsymmetrically.

More specifically, in the substrate 1 of this embodiment, the beveled portions 1a and 1b formed around the circumferential edges of the front and back surfaces have the same beveled widths w_3 and w_4, and the beveled portions 1a and 1b are arranged such that they have different beveled depths d_3 and d_4. The circumferential edges of the substrate provided with the beveled portions 1a and 1b are rounded with the radies of curvatuire of R1 and R2, respectively.

These radies of curvature of R1 and R2 are formed simultaneously when the beveling process is carried out or by a mechanical and/or chemical erosion process independently of the beveling process.

More specifically, the beveled depth d_3 of the front surface is set to such a value that permits a part of the beveled portion to be left after the substrate has been subjected to lapping, grinding for half-off, or polishing. The beveled depth d_4 of the beveled portion 1b is set to such a value that permits a part of the beveled portion to be left when it is lapped. On the other hand, the width w_4 of the beveled portion 1b of the back side is set to a value capable of preventing the chip-off of the substrate 1 or to a value larger than it. The beveled width w_4 is finally determined in relation to the beveled depth d_4. Further, the front beveled width w_3 is made equal to the above beveled width w_4. More specifically, they are set such that the beveled angle θ_3 of the front surface [θ_3 = arc tan(d_3/w_3)] is larger than the beveled angle θ_4 of the back surface [θ_4 = arc tan(d_4/w_4)]. No problem arises even if the beveled angle θ_3 of the front surface is made larger than the beveled angle θ_4 of the back surface, as described above. This is because that since the accuracy of photolithography technology required in the fabricating process of a semiconductor integrated device is not required in the fabricating process of a discrete semiconductor device, it is sufficient only if the beveled portions can prevent the occurrence of chip-off due to a mechanical shock mainly caused in the fabricating process thereof, and a strict profile is not required thereto.

Next, a method of processing the above substrate 1 for semiconductor device will be described with reference to Figure 2.

First, an ingot of a silicon monocrystal is cut in round slices from a cylindrical crystal to provide a substrate 11 for semiconductor device having a prescribed thickness (numeral 11 is used to discriminate this substrate from the substrate 1 for semiconductor device to which the beveled portions 1a and 1b have been formed). Next, the beveled portions 1a and 1b are formed using a grindstone 2 shown in Figure 2.

To describe here the grinding surfaces 2a, 2b, and 2c of the rotary grindstone 2 shown in Figure 2, the configuration of the grinding surfaces 2a, 2b, and 2c of the grindstone 2 has a geometrical agreement with the configuration of the periphery of the substrate 1 for semiconductor device of the embodiment. More specifically, the configuration of the grinding surface 2a, 2b, and 2c of the grindstone 2 is such that the circumferential edges of the substrate 1 of the embodiment fit therewith.

When the above substrate 1 for semiconductor device is ground using this grindstone 2, the substrate 11 is gradually moved in the direction toward the rotary axis of the grindstone 2, while it is rotated in the direction opposite to that of the grindstone 2, whereby the beveled portions 1a and 1b are formed at the circumferential edges of the sub strate 11.

The substrate for semiconductor device 1 of the embodilment is obtained as described above. The obtained substrate for semiconductor device 1 of the embodiment is processed, for example, as follows.

For example, the front and back surfaces of the substrate for semiconductor device 1 are lapped until they reach levels A_1 and A_2, respectively. Further, the front surface of the substrate for semiconductor device 1 is removed (half-off) until a level B is reached, and thereafter the half-off surface is polished. During the time of the course, the outermost rounded portions of the beveled portions 1a and 1b are left as they were.

The following effects can be obtained by the substrate 1 for semiconductor device of the above embodiment and the manufacturing method thereof.

According to the above substrate 1 for semiconductor device, since the angle θ_3 between the inclining surface and the main surface of the front beveled portion 1a (the beveling angle of the front surface) is made larger than the angle θ_4 between the inclining angle and the main surface of the back beveled portion 1b (the beveling angle of the back surface), the thickness of the tip of the periphery of the substrate for semiconductor device 1 is increased and thus the strength of the circumferential edge is increased by the increase in the thickness. As a result, the occurrence of chip-off of the substrate of semiconductor device 1 can be effectively prevented in processes the substrate encounters.

Further, the beveled portions 1a and 1b formed on the front and back surfaces has the same widths w_3 and w_4, and thus when the beveled portions 1a and 1b of the front and back surfaces are simultaneously formed using the grindstone having the grinding surfaces 2a, 2b, and 2c which will fit dimensionally the periphery of the substrate 1 for semiconductor device after it is finished, the edges of the front and back surfaces are simultaneously abutted against the grinding surfaces 2a and 2c of the grindstone 2, whereby the grinding operation thereof is simultaneously carried out and finished at both the edges. As a result, while the beveled portions 1a and 1b are ground, the pressure coming from one of the surfaces being ground is always counterbalancedly that of the other surface being ground, whereby the occurrence of strain due to grinding and the chip-off of the substrate for semiconductor device can be prevented during the operation.

Further, according to the above manufacturing method, since the beveled portions 1a and 1b of the front and back surfaces are simultaneously formed by the grinder 2 having the grinding surfaces 2a, 2b, and 2c which is in a geometrical agreement to the profile of the circumferential edges of the substrate 1 for semiconductor device after it is finished, the edges of the front and back surfaces can be simultaneously abutted against the grinding surfaces 2a and 2c of the grindstone 2, and further the grinding operation is simultaneously carried on and finished. As a result, the occurrence of strain due to grinding and the chip-off of the substrate 1 for semiconductor device can be prevented.

Although the present invention effected by the inventor has been described above in detail with reference to the embodiment, the invention is not limited to the above embodiment, but it is obvious that various modifications can be made within the scope which does not depart from the gist of the invention.

For example, although the beveled portions 1a and 1b are flatly formed in section in the above example, one or both thereof may be formed to have a curved surface of a prescribed radies of curvature in section. In this case, the beveled portions 1a and 1b formed on both main surfaces of the substrate 1 for semiconductor device are formed by curves having different radi of curvature.

The effects provided by the typical inventions disclosed in this application will be simply described below.

According to the present invention, when a substrate for semiconductor device used for a substrate for a discrete semiconductor device is bevelled, the depth of bevelling at the edge to be removed is larger than at the surface that is not removed; the angle between the bevelled surface and the main surface to be removed is larger than the angle of bevelling at the non-removed (back) surface. The bevelling is conducted before or after the dopant in the substrate precursor is subjected to diffusion. By comparison with a substrate in which the angles of bevelling are the same and the

larger of the two different angles, the thickness of the periphery of the substrate is greater, and thus the strength of the circumferential edge of substrate is greater. Chipping is thus reduced or effectively prevented in processes prior to, during or after a half-off process. The bevelled portions formed on both main surfaces of the substrate precursor can have the same width; thus, when the bevelled portions of the removed and non-removed surfaces are simultaneously formed by using a grindstone having a grinding surface geometrically complementing the profile of the periphery of the substrate which is formed, the edges of the removed and non-removed surfaces are simultaneously in contact with the grinding surface of the grindstone, so that the grinding operation is conducted and finished at both edges simultaneously. As a result, the forces exerted at the surfaces being ground are balanced, whereby the occurrence of strain due to grinding and chipping of the substrate can be reduced or prevented.

The novel product, and the precursor used in the process of the invention, may be a silica wafer having bevelled circumferential edges, in which the angles of bevelling are different. Such a product is described and claimed in European Patent Application No. 90304025.1, filed 12.04.90.

Claims

1. A doped substrate (1) suitable for use in or as a semiconductor device, having opposed first and second surfaces each having a circumferential bevelled edge, wherein the concentration of dopant impurities is lower at the first surface that at the second surface, and wherein the angle of bevelling (θ_3) of the first surface is less than the angle of bevelling (θ_4) of the second surface.

2. A substrate according to claim 1, wherein the angles of bevelling (θ_3,θ_4) are substantially different.

3. A substrate according to claim 1 or claim 2, wherein the angle of bevelling (θ_4) of the first surface is less than 30°, 25° or 20°, e.g. about 15°, and/or the angle of bevelling (θ_3) of the second surface is more than 25°, 30° or 35°, e.g. about 40°.

4. A method of making a doped substrate according to any preceding claim, which comprises subjecting the dopant in a doped substrate precursor to diffusion and thereby concentrating the dopant at a surface (the second surface of the doped substrate) thereof; before or after the diffusion, bevelling the substrate precursor; and slicing the doped substrate precursor and polishing the resultant substrate first surface.

5. A method according to claim 4, wherein the bevelled edges of the substrate precursor are formed simultaneously.

6. A method according to claim 4 or claim 5, wherein the widths (W_3,W_4) of the bevelled edges (1a, 1b) of the substrate precursor are substantially the same.

7. A method according to any of claims 4 to 6, wherein the thickness of the periphery ($T-d_3-d_4$) of the substrate precursor is at least one-third, e.g. about one-half, of the thickness (T) of the substrate precursor.

FIG.1

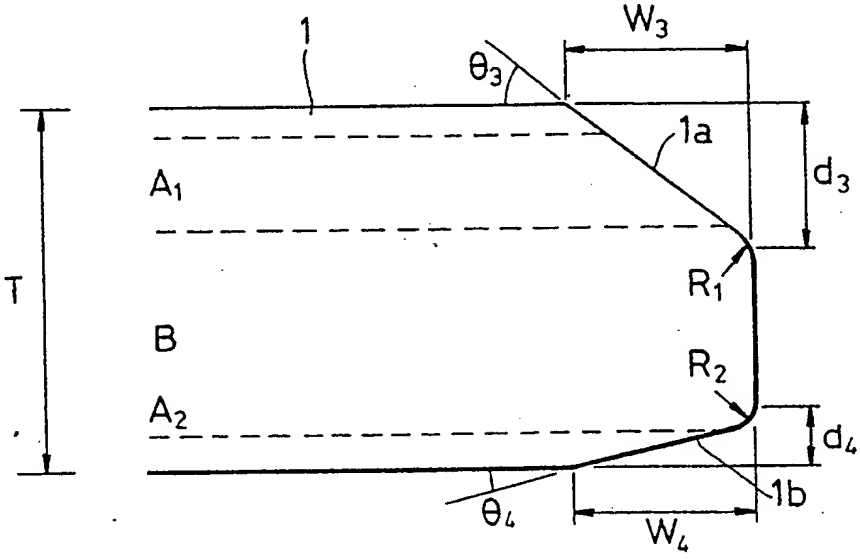


FIG.2

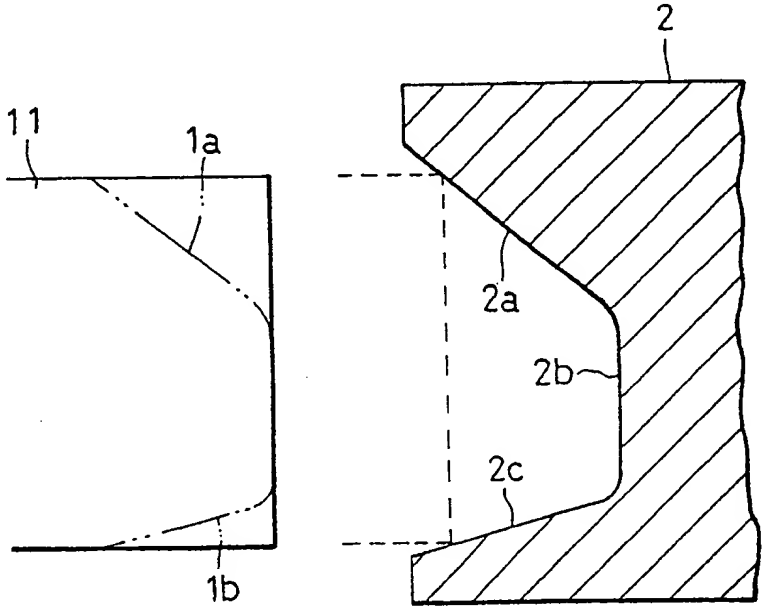


FIG.3

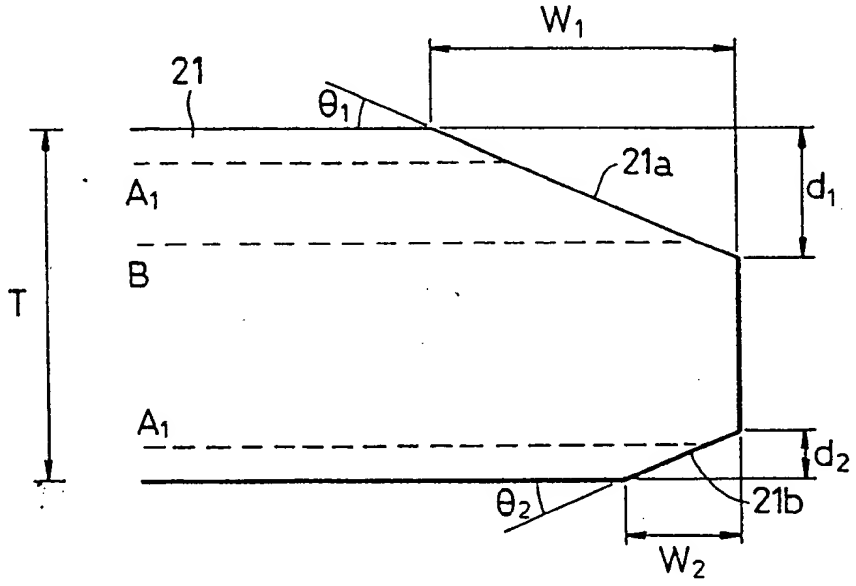
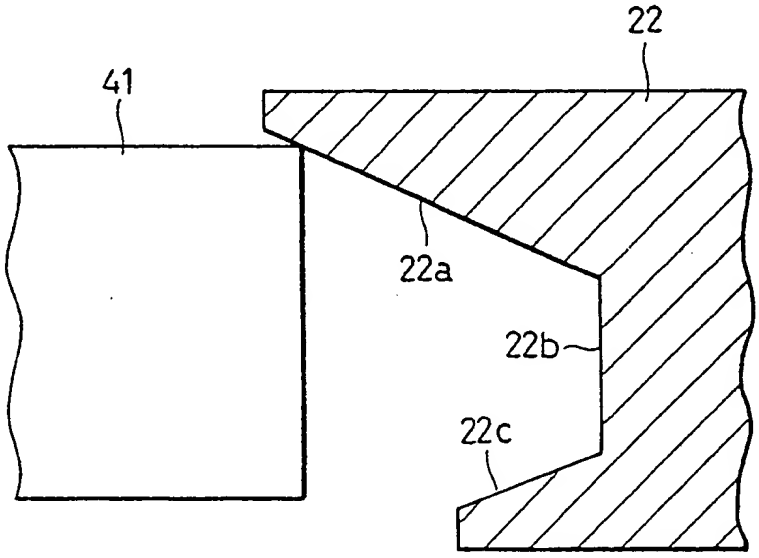


FIG.4



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EUROPEAN SEARCH REPORT

Application Number

EP 90 30 4523

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. ED-31, no. 6, June 1984, pages 733-738, IEEE, New York, US; K.-P. BRIEGER et al.: "The influence of surface charge and bevel angle on the blocking behavior of a high-voltage p+-n-n+ device" * Figures 4,5a *	1-3	H 01 L 21/304
A	US-A-4 630 093 (SUMITOMO ELECTRIC INDUSTRIES) * Figures 3,5 *	1,4,5	
D,A	PATENT ABSTRACTS OF JAPAN, vol. 3, no. 47 (E-105), 20th April 1979; & JP-A-54 024 571 (NIPPON DENKI K.K.) 23-02-1979 * Abstract; figures *	1,4	
A	US-A-3 015 590 (BELL TELEPHONE LAB.) * Figure 4 *	4	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 25, no. 9, February 1983, page 4761, New York, US; E. MENDEL et al.: "Reduction of grinding and lapping defects"	4	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H 01 L
A	FR-A-2 531 108 (HITACHI) * Page 16, line 18 - page 18, line 10; figures 14-15 *	4,5	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	27-08-1990	GELEBART J.F.M.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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